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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/927,368	08/13/2001	Hisaya Mori	50090-332	4507
7590 02/23/2004		EXAMINER		
McDERMOTT, WILL & EMERY		HOLLINGTON, JERMELE M		
600 13th Stree			ART UNIT	PAPER NUMBER
wasnington, 1	DC 20005-3096		2820	

DATE MAILED: 02/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)					
Office Action Commence	09/927,368	MORI ET AL.					
Office Action Summary	Examiner	Art Unit					
	Jermele M. Hollington	2829					
The MAILING DATE of this communica Period for Reply	ation appears on the cover sheet	with the correspondence address					
A SHORTENED STATUTORY PERIOD FOR THE MAILING DATE OF THIS COMMUNICATION - Extensions of time may be available under the provisions of after SIX (6) MONTHS from the mailing date of this communion of the period for reply specified above is less than thirty (30) of the period for reply is specified above, the maximum statuthand in the period for reply with the set or extended period for reply with any reply received by the Office later than three months after earned patent term adjustment. See 37 CFR 1.704(b).	ATION.  37 CFR 1.136(a). In no event, however, may ication.  lays, a reply within the statutory minimum of tory period will apply and will expire SIX (6) M  I, by statute, cause the application to become	a reply be timely filed hinty (30) days will be considered timely.  DNTHS from the mailing date of this communicat  ABANDONED (35 U.S.C. § 133).	tion.				
1) Responsive to communication(s) filed	on <u>06 November 2003</u> .						
2a) This action is <b>FINAL</b> . 2b)							
Since this application is in condition fo closed in accordance with the practice	r allowance except for formal m under <i>Ex part</i> e <i>Quayle</i> , 1935 C	atters, prosecution as to the merits .D. 11, 453 O.G. 213.	is				
Disposition of Claims							
4)⊠ Claim(s) 1-5 and 7-12 is/are pending in	n the application.		·				
4a) Of the above claim(s) is/are	withdrawn from consideration.						
5) Claim(s) is/are allowed.							
6)⊠ Claim(s) <u>1-5 and 7-12</u> is/are rejected.	6)⊠ Claim(s) <u>1-5 and 7-12</u> is/are rejected.						
	)□ Claim(s) is/are objected to.						
8) Claim(s) are subject to restriction	on and/or election requirement.						
Application Papers							
9) ☐ The specification is objected to by the							
10) The drawing(s) filed on is/are: a							
Applicant may not request that any objecti			1(d)				
Replacement drawing sheet(s) including the							
11) The oath or declaration is objected to b	by the Examiner. Note the attack	led Office Action of form 10 102	•				
Priority under 35 U.S.C. §§ 119 and 120		2 5 440(a) (d) ar (f)					
12) △ Acknowledgment is made of a claim for a) △ All b) □ Some * c) □ None of:  1. △ Certified copies of the priority do 2. □ Certified copies of the priority do 3. □ Copies of the certified copies of application from the Internationa * See the attached detailed Office action 13) □ Acknowledgment is made of a claim for since a specific reference was included 37 CFR 1.78.  a) □ The translation of the foreign lang 14) □ Acknowledgment is made of a claim for reference was included in the first senter.	ocuments have been received. ocuments have been received in the priority documents have be al Bureau (PCT Rule 17.2(a)). for a list of the certified copies re domestic priority under 35 U.S. in the first sentence of the speci-	a Application No en received in this National Stage ot received. C. § 119(e) (to a provisional applic fication or in an Application Data S s been received. C. §§ 120 and/or 121 since a spec	sheet. sific				
Attachment(s)							
1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO) 3) Information Disclosure Statement(s) (PTO-1449) Page	O-948) 5) Notice	w Summary (PTO-413) Paper No(s) of Informal Patent Application (PTO-152)	_•				

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## **DETAILED ACTION**

- 1) Note to the applicants, a different examiner is examining this application from now until the application becomes allow or abandon.
  - 2) Claims 1-5 and 7-12 remain for examination.
- 3) The rejection under 35 U.S.C. 103(a) as being unpatentable over Toshishige (01-316024) in view of Rosenthal et al ('521) for claims 1-5, 7 and 10-12 and Toshishige (01-316024) in view of Rosenthal et al ('521) and further in view of Coggins et al ('365) is withdrawn.
  - 4) A new ground of rejection is given as follows.

# Claim Rejections - 35 USC § 112

- The following is a quotation of the second paragraph of 35 U.S.C. 112:
   The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.
- 2. Claims 1-5 and 7-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 1 and 7, the limitation states: "...digital test data produced by converting analog test data output from the digital-to-analog converter circuit into a digital signal..." It is not clear from the claim on how the converting analog test data output from the digital-to-analog converter circuit into a digital signal. It is well known in the art that digital-to-analog converter circuit outputs analog signals only. Even if there are means for producing the output as claimed, the applicants have not described those means within the claim language.

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For examination purposes, the examiner is taking the position that instead of digital test data being produced that analog test data is being produced from an analog signal.

Further claims 1 and 7 states: "... wherein the data memory is divided into two memory sections such that, when digital test data is stored in one memory section, digital test data previously stored in the other memory section is loaded for analysis purpose." It is not clear from the claim how the memory sections are used for analysis purpose. It is not clear from the claim how the applicants determined which section to use and if there could be a switch means to choose which section to use for analysis purpose.

For examination purposes, the examiner is taking the position that the data memory has only one section for analysis purpose until the applicants have given an explanation or modify the claim to explain the memory sections.

Since claims 2-5 depend off of claim 1, they are also rejected for the above reason.

#### Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground

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provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 1 and 7 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 10 of U.S. Patent No. 6,642,736.

Although the conflicting claims are not identical, they are not patentably distinct from each other because although claim 1 of U.S. Patent 6,642,736 does not state that the data memory having two memory sections, it would be obvious of having two section since the test device is testing both D/A converter circuit and A/D converter where, as claimed in claim 1, "...data memory to store the digital test <u>outputs</u>... and... an analyzer portion to analyze each of said digital test <u>outputs</u> stored in said measure data memory..."

## Conclusion

- 5. Applicant's arguments with respect to claims 1-5 and 7-12 have been considered but are most in view of the new ground(s) of rejection.
- 6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Saitoh et al (5436558), Currin et al (5999008), Hashimoto (6255842), Mori et al (6628137 and 6661248) disclose a method and apparatus for testing semiconductor integrated circuit.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (571) 272-1960. The examiner can normally be reached on M-F (9:00-4:30 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (517) 272-1957. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-1651.

Jermele M. Hollington Examiner

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MH

January 29, 2004

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